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side by side			result set
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L29</u>	L26 and l13	1	<u>L29</u>
<u>L28</u>	L26 and l12	81	<u>L28</u>
<u>L27</u>	L26 and l10	112	<u>L27</u>
<u>L26</u>	l15 and (switch\$5 or select\$4 or mux or multiplex\$4 or crossbar\$1)	200	<u>L26</u>
<u>L25</u>	L22 and l13	1	<u>L25</u>
<u>L24</u>	L22 and l12	81	<u>L24</u>
<u>L23</u>	L22 and l10	111	<u>L23</u>
<u>L22</u>	l15 and (switch\$5 or select\$4 or mux or multiplex\$4)	199	<u>L22</u>
<u>L21</u>	l15 and l13	1	<u>L21</u>
<u>L20</u>	l15 and l11	113	<u>L20</u>
<u>L19</u>	l15 and l9	204	<u>L19</u>

<u>L18</u>	l9 and l13	9	<u>L18</u>
<u>L17</u>	l9 and l12	333	<u>L17</u>
<u>L16</u>	l9 and l10	526	<u>L16</u>
<u>L15</u>	l9 and bypass\$4	204	<u>L15</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L14</u>	(710/305-317)[CCLS]	5304	<u>L14</u>
<u>L13</u>	(710/305-317)![CCLS]	5304	<u>L13</u>
<u>L12</u>	(712/201-225,227, 245-248)[CCLS]	6250	<u>L12</u>
<u>L11</u>	(712/2-300)[CCLS]	12886	<u>L11</u>
<u>L10</u>	(712/2-300)![CCLS]	12886	<u>L10</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L9</u>	(fetch\$5 or prefetch\$5 or dispatch\$5 or sequencer\$1) near8 (cycle or period or clock or time) near15 (simultaneous\$3 or parallel\$5 or concurrent\$4)	1613	<u>L9</u>
<u>L8</u>	(fetch\$5 or prefetch\$5 or dispatch\$5 or sequencer\$1) near8 (cycle or period or clock or time)	31780	<u>L8</u>
<u>L7</u>	(by near1 pass\$5 or feedback or feed\$3 near3 back or direct\$4) near12 (arithmetic\$4 or alu\$1 or adder\$1 or subtract\$3 or multipli\$5 or multiply\$5)	93841	<u>L7</u>
<u>L6</u>	(by near1 pass\$5) near12 (arithmetic\$4 or alu\$1 or adder\$1 or subtract\$3 or multipli\$5 or multiply\$5)	19	<u>L6</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L5</u>	6256726.pn.	1	<u>L5</u>
<u>L4</u>	L3 and (prefetch\$5 or fetch\$5 or dispatch\$5)	0	<u>L4</u>
<u>L3</u>	L2 and cycle	1	<u>L3</u>
<u>L2</u>	L1 and (sequenc\$5)	1	<u>L2</u>
<u>L1</u>	4766564.pn.	1	<u>L1</u>

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Collins, J.D.; Tullsen, D.M.;
[Parallel and Distributed Processing Symposium, 2004. Proceedings. 18th International](#)
26-30 April 2004 Page(s):76
Digital Object Identifier 10.1109/IPDPS.2004.1303010
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2. **Energy-efficient register access**
Tseng, J.H.; Asanovic, K.;
[Integrated Circuits and Systems Design, 2000. Proceedings. 13th Symposium on](#)
18-24 Sept. 2000 Page(s):377 - 382
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